Part-A

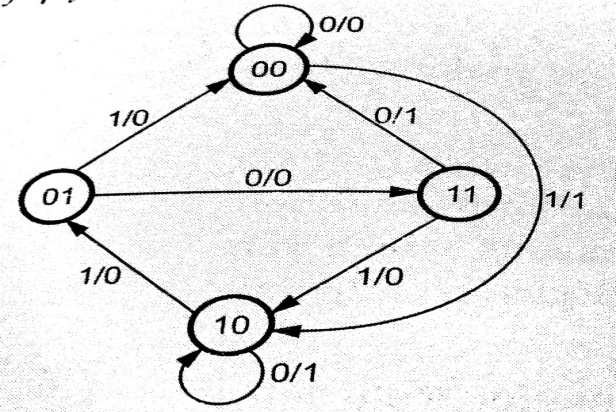
|  |
| --- |
| 1. What are combinational circuits? |
| 1. Define Half subtractor and also draw the logic diagram. |
| 1. List out the application of decoder. |
| 1. Implement the Boolean function using 4:1 multiplexer F(A,B,C)=∑(1,3,5,7) |
| 1. What do you mean by carry propagation delay? |
| 1. Define sequential circuit. |
| 1. Write about the triggering of flip-flop. |
| 1. List out the steps to be followed to design Synchronous sequential circuit. |
| 1. Differentiate between latches and flip flop. |
| 1. What is counter? List out its types. |
| 1. Design half adder using NAND gates. |
| 1. What is parallel adder? |
| 1. Write the design procedure of combinational circuits. |
| 1. Differentiate between Multiplexer and Demultiplexer. |
| 1. Mention the applications of multiplexer. |
| 1. Explain the difference between the performance of asynchronous and synchronous counter. |
| 1. How the Moore circuits differ from Mealy circuit? |
| 1. What is race around condition? |
| 1. Draw the state diagram of SR FF. |
| 1. List out the applications of shift registers |
| 1. What is the function of the enable input in a Multiplexer? |
| 1. Write the design procedure for combinational circuits. |
| 1. What are called don’t care conditions? |
| 1. Can a decoder function as a Demultiplexer? |
| 1. Draw the Implementation diagram of full adder using 2 half adders. |
| 1. What is race around condition? How it can be avoided? |
| 1. Compare synchronous and asynchronous counter. |
| 1. Construct the D flip flop using JK Flip flop. |
| 1. List the basic types of shift registers in terms of data movement. |
| 1. How many flip-flops are needed to build an 8-bit shift register? |

Part-B

1. Design the following multiple output logic circuit using a 4:16 decoder f1=£m(1,2,4,7,8,11,12,13), f2=£m(2,3,9,11), f3=£m(10,12,13,14), f4 = =£m( 2,4,8)
2. Design and implement a full adder circuit using a 3:8 decoder
3. Enforce the full adder circuit using 8:1 multiplexer
4. Implement the following Boolean function using 8:1 multiplexer F(A,B,C,D) = A’B D’+ACD+B’C D+A’C’D
5. Design a 4 bit parallel adder/ subs tractor and draw a logic diagram
6. Design 2 bit comparator using gates
7. Reduce the following function using K-map technique f(A,B,C,D)= £m(0,3,4,7,8,10,12,14)+d(2,6)
8. Minimize the following boolean function- F(A, B, C, D) = Σm(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)
9. Draw and explain the D FFS and T FFS
10. Design a synchronous decade counter using D FFs.
11. Reduce the number of state in the following state diagram. Tabulate the reduced state and draw the reduced diagram.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Present State** | **Next State** | | **Output** | |
| **X=0** | **X=1** | **X=0** | **X=1** |
| A | A | B | 0 | 0 |
| B | C | D | 0 | 0 |
| C | A | D | 0 | 0 |
| D | E | F | 0 | 1 |
| E | A | F | 0 | 1 |
| F | G | F | 0 | 1 |
| G | A | F | 0 | 1 |

1. Design a synchronous counter using SR flip-flop to count the following sequence 0,1,2,4,5,6
2. Explain the working of a master slave JK FF with neat diagram.
3. Design synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop.
4. Design the sequential circuit specified by the following state diagram using D flip flops



1. Design the sequential circuit specified by the following state diagram using T flip flops

